IN THE SPECIFICATION:

Please amend the specification as follows:

Please replace the paragraph beginning on page 1, line 3 with the following amended paragraph:

This application is a continuation of copending application Serial No. 10/266,536 filed October 8, 2002, which itself is a continuation application of application serial number 09/940,660 filed January 24, 2000, now US Patent No. 6,472,897 and assigned to the same assignee, the teachings of which are hereby incorporated by reference.

Please replace the paragraph beginning on page 21, line 5 with the following amended paragraph.

~~Although the drawings depict the test bits are bits 3,5, 7 and 9. As is shown, for test cell~~ In operation, the test bit (T) is directly coupled to the OR gate (via transfer gate 38, described below). Likewise, the above described arrangement of the transistors ensures that if the set bit is 0, the ~~fuse he~~ OR gate 30 preferably has two inputs: a test input and a set input. In the embodiment shown in the figures, the test input, T (generated by register 12) passes through the test cell to the input of the OR gate. ~~Additionally~~